Customer No.: 31561
Docket No.:11141-US-PA
Application No.: 10/605,402

AMENDMENT

To the Claims:

1. (previously presented) A method for fabricating a shallow trench isolation (STI) structure that defines an active area, comprising:

forming a patterned mask layer on a substrate;

forming a doped region in the substrate exposed by the mask layer;

forming a shallow trench down to the doped region in the substrate after the doped region is formed, wherein the shallow trench is formed by using the patterned mask layer as an etching mask and the doped region serves as a detection end point of the etching process; and

filling an insulating material into the shallow trench.

2. (original) The method of claim 1, wherein the step of forming the doped region comprises performing an ion implantation using the mask layer as a mask.

3. (original) The method of claim 1, wherein a conductivity type of the doped region is different from a conductivity type of an active device subsequently formed on the active area.

4. (original) The method of claim 1, wherein a conductivity type of the doped region is P-type or N-type.

Claims 5-10. (cancelled)

11. (previously presented) A method for fabricating a dynamic random access memory (DRAM) cell, comprising:

forming a trench capacitor in a substrate;

forming a buried strap in the substrate connecting with an upper portion of the trench capacitor;

forming a patterned mask layer on the substrate;

performing an ion implantation to form a doped region of a first conductivity type in the substrate exposed by the mask layer;

performing an etching process to etch the substrate down to the doped region to form a shallow trench;

filling an isolating material into the shallow trench;

removing the mask layer;

forming a first doped layer of the first conductivity type in the substrate, wherein the first doped layer is formed at a depth lower than that of the doped region; and

forming an active device on the substrate, the active device being coupled to the trench capacitor via the buried strap.

12. (original) The method of claim 11, further comprising forming a second doped layer of a second conductivity type in the substrate electrically connected with a lower electrode of the trench capacitor, the second doped layer being formed at a depth between the doped region and the first doped layer.

13. (previously presented) The method of claim 11, wherein the doped region of the first conductivity type serves as a detection end point of the etching process.

14. (original) The method of claim 11, wherein the first conductivity type is different from a conductivity type of the active device.

15. (original) The method of claim 14, wherein the first conductivity type is P-type.

16. (original) The method of claim 11, wherein a thickness of the mask layer is larger than 600Å.

17. (original) The method of claim 11, further comprising forming a screen oxide layer on a surface of the substrate after the mask layer is removed.

18. (original) A dynamic random access memory (DRAM) cell, comprising:

a trench capacitor in a substrate, including a lower electrode, an inter-electrode dielectric layer and an upper electrode;

a shallow trench isolation layer in the substrate, having a portion encroaching upon the trench capacitor;

a doped region of a first conductivity type in the substrate directly under a bottom of the shallow trench isolation layer;

a first doped layer of the first conductivity type in the substrate lower than the doped region; and

an active device on the substrate coupled to the trench capacitor.

19. (original) The DRAM cell of claim 18, wherein the first conductivity type is different from a conductivity type of the active device.

20. (original) The DRAM of claim 18, further comprising a second doped layer of a second conductivity type in the substrate electrically connected with the lower electrode of the trench capacitor.

21. (original) The DRAM of claim 20, wherein the first doped layer is disposed at a depth between the doped region and the second doped layer.

22. (original) The DRAM of claim 18, further comprising a buried strap in the substrate connected with an upper portion of the upper electrode of the trench capacitor, the buried strap coupling the trench capacitor to the active device.